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BCA Honours | Semester V | Calicut University

Digital Fundamentals and Computer Organization

Course Code: BCA5CJ303 • Module 4 Notes

MODULE IV: MEMORY HIERARCHY AND CACHE MAPPING

1. Cache Mapping Architectures and TLB Virtual Memory

Cache memory bridges the speed discrepancy between high-speed CPU registers and DRAM main memory via Direct Mapping, Fully Associative, or Set-Associative mapping.

2. Illustrative Computational Working: Step-by-Step Numerical Example

Worked Numerical Example: 4-Way Set-Associative Cache Address Partitioning

Problem Statement:

A computer architecture features a **32-bit byte-addressable physical memory space**. The system employs a 128 KB **cache** with a cache block (line) size of 64 bytes configured as **4-Way Set-Associative**.

Calculate the exact bit allocation for: (a) Byte Offset, (b) Set Index, and (c) Tag field.

Solution & Step-by-Step Working:

1. Byte Offset Bits (w):

Block size = 64 bytes $= 2^6$ bytes$implies$**w** $=$ **6** bits.

2. Total Cache Lines:

$$\text{Total Lines} = \frac{\text{Cache Size}}{\text{Block Size}} = \frac{128\ \text{KB}}{64\ \text{B}} = \frac{131,072}{64} = 2,048\ \text{lines}$$

3. Number of Sets (d):

In 4-Way Set-Associative mode, each set contains 4 lines:

$$\text{Number of Sets} = \frac{2,048\ \text{lines}}{4\ \text{lines/set}} = 512\ \text{sets} = 2^9\ \text{sets}$$

Therefore, Set Index bits $d = \mathbf{9}$ bits.

4. Tag Field Bits (s):

Total physical address width = 32 bits.

$$\text{Tag Bits} = 32 - (\text{Set Bits} + \text{Offset Bits}) = 32 - (9 + 6) = 32 - 15 = \mathbf{17}\ \text{bits}$$

Summary Address Layout:

Field Name	Tag Field	Set Index Field	Byte Offset Field
Bit Width	**17 bits**	**9 bits**	**6 bits**

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Field Name	Tag Field	Set Index Field	Byte Offset Field
Bit Positions	Bits [31:15]	Bits [14:6]	Bits [5:0]

Advanced Architectural Extensions & Industrial Systems Synthesis

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1. Contemporary Engineering Dilemmas and Architectural Solutions

Engineering teams designing software systems centered around Digital Fundamentals and Computer Organization must systematically navigate critical technical trade-offs:

- **Execution Throughput versus Memory Footprint:** In high-performance computational pipelines related to Cache Architecture and Memory Hierarchy, aggressive caching, in-memory collections, and uncompressed intermediate data structures drastically reduce CPU cycle overhead and latency, but expand physical RAM footprint. Conversely, compact serialized representations conserve memory at the cost of continuous decompression overhead. High-throughput architectures deploy off-heap memory buffers and zero-copy data pipelines.
- **Synchronous Simplicity versus Reactive Concurrency:** While synchronous blocking execution models offer straightforward debugging and predictable stack traces, they quickly exhaust thread pool limits under heavy concurrent traffic. Contemporary enterprise frameworks adopt reactive, non-blocking asynchronous architectures (event loops, coroutines, reactive streams) that handle millions of concurrent connections with minimal context switching.
- **Monolithic Cohesion versus Distributed Microservices:** Decomposing large codebases into independently deployable microservices isolates failure domains and enables autonomous team scaling, but introduces network latency, distributed transaction complexities, and eventual consistency challenges.

2. Empirical Comparative Framework

A structured comparative assessment clarifies operational distinctions across conventional and contemporary paradigms in Digital Fundamentals and Computer Organization:

Evaluation Dimension	Conventional Traditional Approach	Contemporary Integrated Paradigm	Strategic Impact Metric
Runtime Execution	Interpreted or single-threaded execution with manual memory management.	Adaptive Just-In-Time (JIT) compilation with generational garbage collection and hardware SIMD acceleration.	High-throughput operational execution with minimal latency jitter.
Data Access Architecture	Direct relational database queries with heavy connection creation latency.	Connection pooling, asynchronous Object-Relational Mapping (ORM), and multi-tier distributed caching (Redis).	Sub-millisecond query responses and resilient database load protection.

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3. Step-by-Step Implementation and Operational Governance Roadmap

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Industrial Risk Governance, Statutory Compliance & Failure Mode Analysis

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Statutory & Regulatory Risk	Violations of data privacy standards (DPDP Act, GDPR), unencrypted customer data storage.	Unencrypted database backups, audit logging gaps during user credential changes.	End-to-end data encryption (AES-256), strict role-based access control, automated regulatory compliance auditing.

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